



Benefits

- Allows rapid development of defense applications, saving you internal development effort and enabling you focus on higher level integration issues
- Eliminates integration problems through ordering as part of an integrated SDR-2000, SDR-3000, SDR-4000 or HCDR-1000 series platform
- Off-the-shelf Intellectual Property (IP) cores reduce cost and development time for programs requiring high performance frontend processing applications that optimize the platform for speed, power, and size

Applications

- Military Communications/Tactical MILCOM
- Electronic Countermeasures
- Electronic Support Measures
- Signals Intelligence (Wideband Spectral Analysis, Multichannel Direction Finding)
- Phased Array Surveillance RADAR
- Wireless Data Link
- Satellite Communications

Description

To maximize the processing capabilities of a *flexComm*[™] software defined radio platform, Spectrum offers field programmable gate array (FPGA) Intellectual Property (IP) cores integrated onto its platform. The cores offer wide-band capability, good dynamic range and low-level signal accuracy to fulfill some of the key requirements in defense electronic design. Using off-the-shelf IP cores enables internal design teams to concentrate on high-level integration issues and can reduce the cost and development risk relative to designing in-house.

These IP cores are designed using advanced modeling tools that optimize fixed-point implementations resulting in minimum silicon and least power consumption - particularly relevant for airborne and mobile applications. The cores address broad system issues such as analog to digital conversion, frequency planning, analog pre-filtering and its overall effect on the digital receiver performance.

[System Design Example]

A typical example of a direction finding (DF) system uses 4 or 6 channel digital inputs, with each channel running at over 100 MS/s. Each channel requires initial filtering and then processing through a real-time FFT, Polyphase discrete Fourier transform (DFT), followed by conversion to power and possible averaging stages before processing in a digital signal processor (DSP). DF system developers can produce this type of design in less than 4 weeks by using these highly flexible off-the-shelf cores.

Features

- Dual 16K point Fast Fourier Transform (FFT) core with sample rates up to 400 MS/s
- Tunable multi-channel receiver cores: Polyphase filter core with 78 channel downconversion at 25 KHz bandwidth using less than 40% of an XC2V6000, and tunable multi-channel downconverter cores with tunable bandwidth and frequency
- 32K point FFT core: Low-cost off-the-shelf FFT cores for Xilinx and Altera FPGA, with sample rates up to 400 MS/s complex, and lengths up to 128k complex points
- Distributed half band filter (DHBF) core: Highly optimized half band, third band, and Nth band filters, for simultaneously filtering, down-converting and decimating a real input signal
- Fixed-point to floating-point converter core: Convert fixed-point data values to single precision floating point format

Intellectual Property Cores

Customers can order the IP cores listed below and Spectrum will integrate the cores onto your *flexComm* platform.

[Dual 16K Point FFT Core]

Key applications: signals intelligence, communications intelligence, direction finding.

There is a range of high specification FPGA-based pipelined FFT cores available that are intended for use in applications where processing speed is critical and optimum use of silicon is required. The pipelined or streaming architecture ensures that all cores can process back-to-back blocks of time-domain input data in real-time. FFT parameters such as radix, processing parallelism and bit growth can be tailored to suit each application resulting in the most optimal design in terms of silicon, power and performance.

The dual 16K point FFT core incorporates a DHBF, a pipelined FFT with a Blackman Window and bit reverser. These cores can be used for signals intelligence, communications intelligence, and direction finding applications.

Features

- Dual channel FFT core with digital half-band filter with 14 bit input
- Blackman Window Function
- Bit reverser
- Dual channel output (I&Q format) with output resolution of 20 bits
- 26-bit internal arithmetic
- Maximum sample rate of 100 MS/s per input channel

[FFT Core Range]

Key applications: wide band filter banks, communications systems, electronic warfare (radar, sonar, surveillance), medical instruments, spectral analysis, multi-channel (many low speed channels can be interleaved through the single high speed core), orthogonal frequency division multiplexing (OFDM) systems.

The FFT cores implement a pipelined radix-2 decimate in frequency (DIF) algorithm with a parallelism of 4. These cores can typically accept complex time-domain data at a maximum continuous rate of 400 MS/s.

Features

- Proven in Xilinx and Altera
- Continuous real-time processing up to 400 Msps complex "off-the-shelf" and Gsps "to order"
- 8 to 128k points available in single chip solutions, 4 million points with external to FPGA memory
- Optimized for the speed silicon trade off
- Twiddle width and bit growth adjustable (factory setting)
- Internal memory adjustable at factory
- Fully pipelined design

[Tunable Multi-Channel Receiver Cores]

Key applications: software defined radio, digital down converter replacement, communications systems, multi-standard flexible base station, electronic warfare (including radar, sonar, surveillance), real-time spectral analysis, selective power measurement, medical instruments.

Two tunable multi-channel receiver cores are available. The polyphase filter provides great density and efficiency for the downconversion rate per gate and operates at a constant bandwidth. This core can produce a 78 channel downconversion at 25 KHz bandwidth using less than 40% of an XC2V6000.

A tunable multi-channel downconverter is also available and allows both tunable bandwidth and frequency. This footprint is slightly larger but provides a completely configurable core.

[Distributed Half Band Filter Core]

Key applications: digital downconverter replacement, high speed front-ends.

The DHBF is a 'downconvert and decimate' filter, primarily intended for use as the first stage in very high sample rate DSP systems. Data is presented at the DHBF input from a high speed sampling system (typically an anti-aliasing filter and A-to-D) and the input signal is downconverted to base-band with the frequency range $\pm f_s/4$ (where f_s is the input sample rate).

The DHBF architecture is implemented onto an FPGA device to optimize speed and silicon usage, depending on the customers design parameters. Half band filter characteristics can be specified over a wide range with regard to side-lobe (stop-band) level and filter order. Higher order (sharper) filters will typically increase silicon usage, but the flexible architecture of the DHBF will minimize silicon usage for implementation.

Features

- Proven in Xilinx and Altera devices
- Easy migration to most FPGA vendors' devices and architectures
- Half band filter can be specified for stop-band attenuation and filter order
- Provides a high performance front-end for the Polyphase or FFT architectures
- Various data input bit widths can be implemented
- Fully synchronous design

[Fixed-to-Floating Point]

Key application: FPGA to DSP interfacing

In many system designs using fixed-point processing, the FPGA output bit width can become quite large and is often not in a format desirable for the following stages of the system. Integer-to-floating point conversion cores can overcome this issue. In this specific example, a 64-bit signed integer to IEEE-754 32-bit single precision floating-point format converter core can be used. The core is provided in EDIF netlist form as a component.

The core converts 64-bit signed integer input values into 32-bit IEEE-754 single precision output values. The conversion process is pipelined so that a continuous series of values can be converted at the clock rate applied to the core. A 'NaN' (Not a Number) control input is provided to force the output of the core to a NaN value of all ones. This feature may be used to provide a unique 'sync' or 'idle' value that can be easily interpreted by down-stream processes

Features

- Proven in Xilinx and Altera devices
- Easy migration to most FPGA vendors' devices and architectures
- Other data formats can be implemented
- Fully synchronous design

[Licensing]

FPGA IP cores are licensed to the device type, and are not associated with a particular Spectrum platform. A license must be purchased for each instantiation of the core on an FPGA. For example:

- If a core will reside in each of the 4 FPGAs on a PRO-3100, then 4 licenses must be purchased
- If a core will reside multiple times on a single FPGA, then multiple licenses must be purchased

Delivery of cores include:

- EDIF net list file with warranty certifying it meets the written specification
- User constraints file
- VHDL instantiation template
- VHDL test bench including ModelSim script and test data files, compiled RTL VHDL Model, bit-true Matlab model and scripts, and placement reports

Licensing terms include the delivery of a net list for the core products that has a warranty certifying that it meets the written specification. The warranty period is usually 90 days. A single use license can be purchased for prototyping and then upgraded to a higher number of uses at deployment time. Standard price breaks are at 1, 10, 50, and 1000 uses. Quantities above 100 uses are negotiated on an individual basis. Additional support contracts can be provided to cover modifications and support for the specified core design.

[Order Information]

Please contact your Spectrum Sales Representative.