

IS THERE REALLY SUCH A THING AS A “DSP” ANYMORE?

If you read a broad collection of trade journals and magazines focused on wireless communications, in any given month you are likely to find a number of articles discussing the use of different types of “off-the-shelf” digital signal processing devices in wireless systems. The types of devices generally discussed in these publications include application-specific standard products (ASSPs) targeted at wireless communications along with the usual array of programmable devices: field programmable gate arrays (FPGAs), digital signal processors (DSPs), and general-purpose processors (GPPs). I was discussing just such an article with a colleague of mine recently, and he pointed out that, over the past several years, the “type names” for these latter devices have become almost meaningless, stating “there really isn’t any such thing as a DSP anymore.” This was, I felt, a very interesting comment, and worth exploring a bit further.

Consider the following: Wireless original equipment manufacturers (OEMs) are in business to make money. The way they generally make money is by producing products that they can sell copies of at a margin that offsets both the cost of development and the cost of goods sold at a sufficient level to generate a positive return on investment (Fig. 1). Historically, a key mechanism for minimizing cost of goods sold in a wireless device or system has been through the use of application-specific integrated circuits (ASICs) providing fixed or partially programmable functionality for intermediate frequency (IF) and baseband signal processing [1, 2]. These circuits may be provided by a commercial-off-the-shelf device manufacturer in the form of an ASSP, or developed by an OEM’s in-house ASIC design team to be power and cost optimized to support a product’s specific feature set. In products utilizing ASIC-based signal processing technology, off-the-shelf programmable signal processing devices such as DSPs or FPGAs are generally relegated to a supporting role, if used at all, as these devices add to the overall size, weight, power, and cost of the product.

However, DSP and FPGA device manufacturers are also in business to make money. The way they make money is by getting their devices “designed into” products OEMs plan to produce in large volume. What this means is that the programmable device manufacturer’s primary competitors are ASSP device manufacturers and their customer’s own in-house ASIC design teams. So how does a programmable device manufacturer differentiate against these competitors?

For wireless infrastructure systems that ship in lower volume, such as satellite hubs or WiMAX gateways, the answer is driven by the technical complexity inherent in the product. The development cost of these systems is often quite large and must be amortized across a relatively small number of production units. As such, the cost of developing an ASIC in-house would have a significant impact on the overall return on investment, making the use of off-the-shelf signal processing technologies attractive. This saves the OEM the cost of an expensive ASIC development cycle and allows the OEM to get its wireless infrastructure product to market faster.

The development cost of an ASIC also impacts the ASSP manufacturer in supporting wireless infrastructure systems. The requirements of these complex systems tend to vary significantly from product to product, often requiring a new or modified

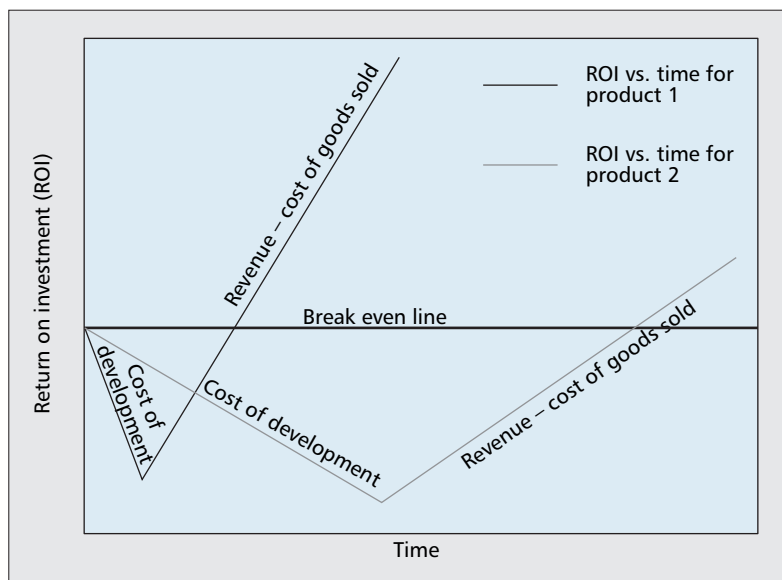


Figure 1. Conceptual model comparing ROI profile for two different wireless systems.

signal processing architecture for each application. This makes it difficult for an ASSP manufacturer to achieve cost reduction through economies of scale in developing application-specific devices that will be utilized by multiple OEMs in creating complex products. The value proposition programmable device manufacturers bring for these types of complex systems, therefore, generally lies in having off-the-shelf devices that are able to support a wide range of system requirements and air interface standards as demonstrated through “reference designs.” This allows the programmable device manufacturers to compete with ASSP providers on cost, since the programmable nature of these devices allows them to be used by multiple different OEMs in multiple different types of systems.

In supporting these complex systems, a variety of programmable signal processing devices are generally required: FPGAs for high-performance front-end signal processing, DSPs for baseband modem processing, and GPPs for control functions and higher-level link and network layer processing [3]. This becomes problematic in high-volume products. For these types of products, such as cellular handsets and mobile satellite terminals, the costs associated with the development of an ASIC can be amortized over thousands of production units, and as such the cost of development is fairly insignificant when compared to cost of goods sold throughout the product’s life cycle. Thus, for high-volume products, the production costs and power dissipation associated with utilizing a mix of FPGA, DSP, and GPP devices is prohibitive when compared to utilizing an ASIC whose features are optimized for that product.

So again, the question is: how does a programmable device manufacturer differentiate against ASIC competition? The strategy a number of these companies have embraced over the past several years is to integrate the capabilities of each class of processor into a single programmable device. The resulting multicore “system on a chip” device is generally optimized to support the IF and baseband processing requirements for a target class of applications within the wireless market and typically includes elements such as:

(Continued on page 36)

(Continued from page 34)

- Front-end analog-to-digital and digital-to-analog converter interfaces
- Programmable logic supporting temporal synchronization on a wireless network
- One or more programmable signal processing elements supporting the algorithmic requirements of modem processing
- A general-purpose processor core supporting link and network layer processing, waveform setup, and control
- Hardware accelerator cores, such as a turbo decoder, supporting common functions that require relatively high performance
- Peripheral input/output (I/O) device interfaces for:
 - Memory
 - Payload data ingress and egress
 - Interaction with the rest of the radio system

Examples of this convergence abound. “FPGA manufacturers,” including Xilinx,[®] Altera,[®] QuickLogic,[®] Lattice,[®] and Atmel[®], have all begun adding elements such as GPP cores, dedicated DSP engines and application-relevant I/O to their device offerings, reducing or eliminating the need for independent DSP or GPP devices in products incorporating their technology [4–8]. Similarly, “DSP manufacturers” such as Texas Instruments[™] and Analog Devices[®] have begun incorporating wireless instruction sets, hardware accelerators, GPP cores, and application-relevant I/O to their device offerings, reducing or eliminating the need for independent FPGA or GPP devices in products incorporating their technology [9–11]. In addition, companies such as Broadcom[®] and Freescale[™] are integrating DSP cores from StarCore[™] and Ceva[™] with GPPs, hardware accelerators, and I/O to create baseband processors targeted at wireless communications that compete directly with the offerings of the more traditional device vendors [12–15]. Finally, a number of newer companies, such as picoChip, have also gotten into the act, again integrating their proprietary high-performance DSP engines with GPPs, hardware accelerators, and I/O to create baseband processors targeted at wireless communications [16].

By integrating these various technologies into a single programmable “system on a chip,” device manufacturers can create a family of off-the-shelf products that begin to become size, weight, power and cost competitive with competing ASIC technologies [17]. This includes not only devices developed in-house by OEMs for specific products, but also ASSP devices from companies such as QUALCOMM[®] incorporating a mix of fixed function air interface processors with programmable processors for use in cellular handsets [18]. The ability to compete is especially true for wireless products that must support multiple air interface standards, such as cellular, WiFi, and WiMAX, since different fixed function application-specific processors are typically required for each wireless protocol stack. For these types of terminals, a single programmable device can often replace multiple application-specific processors by “loading” the application code for the desired air interface dynamically while the handset or terminal is in operation. This capability of programmable devices has the potential to dramatically reduce the overall cost of the handset and potentially increase battery life by eliminating the static power dissipation associated with multiple application-specific technologies. The nature of these programmable devices also offers the added benefit of allowing new revenue generating features and capabilities to be added to the wireless product while it is in service.

So, is there such a thing as a DSP anymore? Well, the short answer is yes, but the use of a traditional signal processing device like a DSP is typically limited to lower-volume complex wireless systems, with higher-volume wireless products tending toward the use of more integrated programmable system on a chip technologies. The emergence of these multicore devices combining the functionality of ASSPs, GPPs, DSPs, and FPGAs into a single offering complicates the design choices in radio systems. The development team for any new advanced wireless product must now spend considerable effort evaluating whether a radio function traditionally performed on an ASIC would, for example, be better implemented on an FPGA supporting integrated DSP and GPP cores or on a DSP with integrated wireless IP and GPP cores. Looking forward, design choices will likely become even more difficult, with FPGA and DSP vendors competing with each other head-on in the various segments of the wireless market. Where will this end? Well, the logical progression of this technology is to multiband multimode “radio on a chip” devices integrating an RF front-end core into the system on a chip device for further size, weight, power, and cost savings. While it is reasonable to assume that we are years away from the broad adoption of off-the-shelf radio on a chip products, the trend toward integrated technologies is clear, allowing off-the-shelf programmable device manufacturers to compete more and more with in-house ASIC design teams for the IF and baseband signal processing technology incorporated into wireless products.

REFERENCES

- [1] MorphICs Technology Inc., “Smart Signal Processing for 3G Wireless Communications,” <http://www.morphics.com/technology>
- [2] L. Pucker, “Paving Paths to Software Radio Design,” http://www.comms-design.com/csdmag/sections/cover_story/showArticle.jhtml?articleID=16502928
- [3] L. Pucker, “Design Considerations for Distributed Architecture Software Defined Radios,” *Proc. Commun. Des. Conf.*, Sep. 2002
- [4] Xilinx, “Platform Studio Product Brief,” http://www.xilinx.com/bvdocs/ipcenter/data_sheet/EDK_Sell_Sheet.pdf
- [5] Altera, “SOPC Builder Product Brief,” <http://www.altera.com/products/software/products/sopc/sop-index.html>
- [6] QuickLogic, “QuickMIPS Product Brief,” http://www.quicklogic.com/images/QuickMIPS_QL90xM_PB.pdf
- [7] Lattice Semiconductor, “LatticeSC FPGA Family Product Brief,” http://www.latticesemi.com/documents/SC_pb.pdf
- [8] Atmel, “FPSLIC[™] (AVR with FPGA) Product Overview,” <http://www.atmel.com/products/FPSLIC/overview.asp>
- [9] Texas Instruments, “OMAP3430 multimedia applications processor,” http://focus.ti.com/pdfs/wtbu/ti_omap3430.pdf
- [10] Texas Instruments, “TMS320TC16482 High Performance, Low Power, Programmable DSP for Wireless Base Stations”, <http://focus.ti.com/lit/ml/sprt346/sprt346.pdf>
- [11] Analog Devices, “2006 Wireless Handset IC Selection Guide,” http://www.analog.com/UploadedFiles/Product_Highlights/13674581406_Catalog14LR.pdf
- [12] StarCore, “StarCores’s SC140 DSP Core,” http://www.techonline.com/community/related_content/13080
- [13] CEVA, “CEVA-Teaklite Product Note,” http://www.ceva-dsp.com/products/cores/pdf/ceva-teaklite_datasheet.pdf
- [14] Broadcom, “BCM2152 Product Brief,” <http://www.broadcom.com/collateral/pb/2152-PB03-R.pdf>
- [15] Freescale Semiconductor, “i.300-30 Innovative Convergence Platforms Fact Sheet,” http://www.freescale.com/files/platforms/doc/fact_sheet/I30030INCNPFS.pdf
- [16] R. Baines and D. Pulley, “A Total Cost Approach to Evaluating Different Reconfigurable Architectures for Baseband Processing in Wireless Receivers,” *IEEE Commun. Mag.*, vol. 41, no. 1, Jan 2003, pp. 105–113
- [17] D. Bursky, “Designers stretched in ASIC, FPGA tug-of-war,” *Elect. Eng. Times*, May 1, 2006 pp. 45–52
- [18] QUALCOMM, “MSM7500 Chipset Solution,” http://www.cdmatech.com/download_library/pdf/msm7500_chipset.pdf